the channel region and the semiconductor region via a gate insulator, a thickness of a gate insulator being constant, and the side-wall gate portion being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region; and

a side-wall insulating film provided on a side surface of the gate electrode and the side surface of the convex semiconductor layer.

Concld C1

**IN THE DRAWINGS:**

Submitted herewith is a Request for Approval of Drawing Changes in which Applicant proposes amending Figs. 79-81 to add the legend "Prior Art."

## REMARKS

By the present Amendment, Applicant proposes amending claims 1 and 2 to more appropriately define the invention, and proposes amending the drawings as indicated in the Request for Approval of Drawing Changes filed concurrently herewith. Claims 1-21 and 23-45 are pending, with claims 3-21 and 24-34 being withdrawn from further consideration by an election of species.

In the Office Action, the Examiner objected to the drawings and rejected claims 1, 2, 23, and 35-45 under 35 U.S.C. § 103(a) as unpatentable over Miyawaki et al., U.S. Patent No. 5,567,962 ("Miyawaki"). Applicant respectfully traverses the objection and rejection for the following reasons.

**Objection to the Drawings**

The Examiner objected to the drawings. As required by the Examiner, Applicant proposes amending the drawings in the Request for Approval of Drawing Changes filed

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concurrently herewith to add the legend "Prior Art" to Figs. 79-81. Therefore, Applicant respectfully requests that the objection to the drawings be withdrawn.

**Rejection Under 35 U.S.C. § 103(a)**

The Examiner rejected claims 1, 2, 23, and 35-45 under 35 U.S.C. § 103(a) as unpatentable over Miyawaki.

Upon entry of this Amendment, claim 1 will recite, *inter alia*, "a gate electrode having a side-wall gate portion provided over a side surface of [a] convex semiconductor layer, the gate electrode applying an electric field effect to [a] channel region and [a] semiconductor region via a gate insulator, a thickness of the gate insulator being constant, and the side-wall gate portion being offset with respect to a part of a lower portion of [a] source region and a part of a lower portion of [a] drain region" (emphasis added). Claim 2 will also include, *inter alia,* recite similar recitations.

Miyawaki is directed to a semiconductor memory device. Miyawaki discloses that the device comprises a substrate 1012, a gate electrode 1023, an impurity region 1016, and a gate insulator 1022. Miyawaki, Fig. 12. In contrast to claims 1 and 2, Miyawaki discloses that the thickness of the gate insulator 1022 in the part where the region 1016 and the gate electrode 1023 are opposed to each other is not constant, but increases in thickness. *See* Miyawaki, Figs. 12, 13. This occurs because of the formation method of Miyawaki. Miyawaki discloses that the element separation region is formed using the LOCOS method. *See* Miyawaki, Fig. 32. Consequently, a "Bird's break" is formed in that part of the gate insulator 1022 where the region 1016 and the gate electrode 1023 are opposed to each other. Therefore, the thickness of the gate

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insulator 1022 is not constant. Rather, the gate insulator increases in thickness at the lower portion of the gate.

Thus, Miyawaki fails to teach or suggest at least "a thickness of the gate insulator being constant." For at least this reason, claims 1 and 2 are allowable. Claims 23 and 35-44 are allowable at least due to their dependence from allowable claim 1 and claim 45 is allowable at least due to its dependence from allowable claim 2.

One advantage of embodiments consistent with the present invention is control of a punch-through between a source and a drain. Punch-through voltage occurs when an electric current flows through a depletion layer formed between the source and the drain. Punch-through arises when there is a potential difference between the source and the drain, and the potential of the gate electrode is, for example, 0V, i.e., when the transistor is OFF. When potential reaches a certain level, an electric current flows through the depletion layer. This electric current is called a punch-through current. The cut-off characteristic of a transistor depends on the intensity of the punch-through current.

The punch-through current flows through the region where it is most difficult for the potential from the gate electrode, 0V, for example, to reach. In other words, it is the region between the lower portion of the drain and the lower portion of the source in a transistor including a convex semiconductor region. The cut-off characteristic of this type of transistor may be improved by suppressing the punch-through phenomenon, thereby lowering the punch-through current. This can be achieved by making it easier for the potential from the gate electrode to reach the region where the punch-through current flows. Accordingly, the thickness of a gate insulator may be made constant in

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this region. Thus, the potential from the gate electrode reaches the region where the punch-through current flows.

**Conclusion**

Applicant respectfully requests that this Amendment under 37 C.F.R. § 1.116 be entered by the Examiner, placing claims 1, 2, 23, and 35-45 in condition for allowance. Therefore, this Amendment should allow for immediate action by the Examiner.

Furthermore, Applicant respectfully points out that the final action by the Examiner presented some new arguments as to the application of the art against Applicant's invention. It is respectfully submitted that the entering of the Amendment would allow the Applicant to reply to the final rejections and place the application in condition for allowance.

Attached hereto is a marked-up version of the changes made to the title, specification, claims, and abstract by this Amendment. The attachment is captioned "**Appendix to Amendment of December 24, 2002**".

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: December 24, 2002

By: Robert J. Rotella Reg. No. 24,014
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## Appendix t Amendment of D cemb r 24, 2002

**IN THE CLAIMS:**

Please amend claims 1 and 2 as follows:

1. (Twice Amended) A semiconductor device comprising:

a convex semiconductor layer provided on a semiconductor substrate;

a source region and a drain region provided in the convex semiconductor layer; [and]

a semiconductor region having an impurity concentration higher than that of a channel region provided between the source and drain regions, the semiconductor region provided between the semiconductor substrate and the source region, between the semiconductor substrate and the drain region, and between the semiconductor substrate and the channel region, respectively; and

a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, [in an insulated state with respect to the convex semiconductor layer,] the gate electrode applying an electric field effect to [a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer,] the channel region and the semiconductor region via a gate insulator, a thickness of the gate insulator being constant, and the side-wall gate portion being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region.

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2. (Amended) A semiconductor device comprising:

a convex semiconductor layer provided on a substrate;

a source region and a drain region provided in the convex semiconductor layer;

a semiconductor region having an impurity concentration higher than that of a channel region provided between the source and drain regions, the semiconductor region provided between the semiconductor substrate and the source region, between the semiconductor substrate and the drain region and between the semiconductor substrate and the channel region, respectively;

a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, [in an insulated state with respect to the convex semiconductor layer,] the gate electrode applying an electric field effect to [a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer] the channel region and the semiconductor region via a gate insulator, a thickness of a gate insulator being constant, and the side-wall gate portion being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region; and

a side-wall insulating film provided on a side surface of the gate electrode and the side surface of the convex semiconductor layer.

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